Thermal Management Challenges for 3D Packaging

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Outline

- Need, Evolution and Proliferation of 3D packaging
  - Moore’s Law and Packaging
  - Density and Power
  - Miniaturization and Performance
  - Cost

- Thermal Management of 3D Packaging
  - Stacked Chip Package
    - Traditional interconnect (WB, FC)
    - Through silicon via

- Summary and Conclusion
Moore’s Law and packaging

- The industry has been able to keep pace with Moore’s Law by shrinking transistors.
- Limitations to transistor gate size are an issue in the future and interconnect losses pose a serious problem for high speed chips now.
- 3D packaging provides increased density and performance and is a key element to meeting/exceeding Moore’s predictions.
Density and Power

- In the last decade chip stacking has been used as a way to increase density using like and mixed die sets.
- The proliferation of powerful mobile devices has continued to test the limits of density and performance in compact systems.
- More power in smaller spaces.
- Consumer demand for higher performance and smaller form factor continues.
- Stacked chip packaging is a primary enabler for these devices.
- Thermal management issues are core to the success of a given multi-chip design.
Miniaturization and Performance

- High performance computing is limited by interconnect losses
- Interconnect scalability cannot keep pace with gate length
- Interconnect switching power can be 50% of overall dynamic power
- Stacking chips can reduce chip-to-chip interconnect length but does not address on-chip interconnect length
- Through-silicon vias help to reduce interconnect losses on-chip and chip-to-chip
Cost

- Reducing cost or maintaining cost with more functionality is the number one priority.
- Stacking packages and chips may be less costly than advancing lithography.
- TSV and other 3D packaging technologies reduce real estate, material usage and back-end process costs.
Stacked Package Examples

- Stacked-SiP
- 4 S-CSP
- 3-die SCSP thin spacer tech
- PTP
- etCSP Stack

- Fold over TABGA Pckg Stack TSLGA
- TABGA/TSLGA with Discrete Flex Arms
- Fold over TABGA Integrated Flex Arm
- S-etCSP / FSTABGA (integrated flex arm)
- TSBGA on FCBGA

3,4 Die Fold μBGA
3D Packaging

Toshiba MCP

4 Die μZ® Ball Stack  8 Die μZ® Ball Stack

Tessera uZ Ball Stack Package

Elpida Memory Tape Carrier Package

STEC TSOP Stacking

www.bit-tech.net
3D Packaging

Assembled Package-on-Package

Package-on-Package (PoP)

Top Package - Integrates high capacity memory device by die stacking
Bottom Package - Integrates high-density digital logic devices (processor)

Frost and Sullivan

AMD
Chip Stacking
Extreme Chip Stacking

Elpida Memory 1.4mm MCP with 20 Stacked Dies
Thermal Management of Stacked-Chip Packaging
3D Thermal Management

- It is easy to see that in 3D designs, thermal management can be a challenge.
- Chips can’t always be placed in a particular order without the use of spacers.
- Spacers increase thermal resistance and add low-k adhesive layers.
- Care must be taken not to align hot spots.
- Heat removal in traditional packages is provided by external heat sinking, either through the top or the bottom or both.
Stacked Chip Package Thermal

- Plastic overmolded package with 5 chips
  - Logic, memory, special function
  - Varied die size dictates stacking order
  - Chip on bottom of package (cavity)
  - 1.2W total power dissipation
  - TA = 22°C
Stacked Chip Model Results

- FEM Models in SolidWorks COSMOS
- Simple block models include die–attach material thermal resistance and bulk heat transfer coefficients
- Show the effect of heat sinking

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TSV Roadmap
TSV Thermal

- TSV stacked chips pose a unique thermal management challenge
- The fine Cu pillars help to move heat vertically through the stack
- Gaps are introduced that must be filled
- Peripheral TSV are typical but arrays of vias are being investigated to increase heat flow
- Flexibility in placement of arrayed vias will be highly dependent on chip layout and density
**TSV Thermal**

- Gaps are introduced that must be filled
- Peripheral TSV are typical but arrays of vias are being investigated to increase heat flow
- Due to the small size of TSV, computer modeling requires sub-modeling techniques
Thermal Management for TSV

- Use high-thermal conductivity interlayer adhesives / fillers
- Rotate chips such that hot spots are not spatially aligned
- Use materials that protrude from the ‘stack’ and provide direct attachment to heat removal structure
- Add multiple Cu TSV’s to stack
- High thermal conductivity interposer between chips
- Microchannel cooling
Summary

- 3D Packaging is enabling a new generation of high density devices
- Challenges exist in design, process, materials and characterization
- Thermal Management is a primary concern
- Methods must be developed to measure and specify 3D package thermal parameters
TSV and Stacked Thermal Issues

- Thermo–electrical issues
  - Speed / propagation of chips with different temperatures
  - Change in via capacitance due to electrical field strength in Si

- Thermo–mechanical issues
  - Placement of TSV near actives can compress or expand gate
  - CTE mismatch may cause cracking or delamination
THANK YOU!

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